black hat
MIDDLE EAST AND AFRICA

CPU Fuzzing:
Automated Discovery of Microarchitectural Attacks

15 - 17 NOVEMBER 2022
RIYADH FRONT EXHIBITION CENTRE
SAUDI ARABIA

Daniel Weber, Michael Schwarz, Moritz Lipp

CO-ORGANISED BY:

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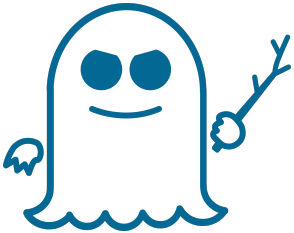

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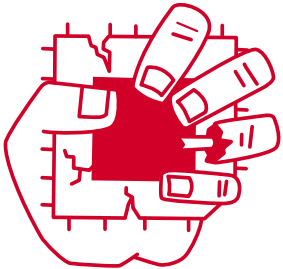

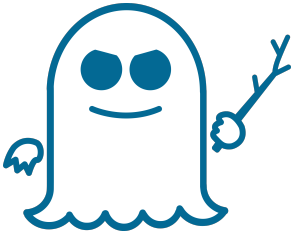


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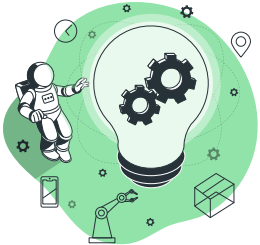
Microarchitectural attacks

Microarchitectural attacks

How do they **work**?

Microarchitectural attacks

How do they **work**?



How can we
find them **efficiently**?

Who am I?

Daniel Weber

PhD Student @ CISPA Helmholtz Center for Information Security

Research on CPU Security and Side Channels

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Who am I?

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Who am I?

Moritz Lipp

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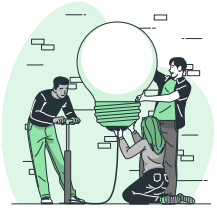
mlipp@amazon.com

Team



Osiris Research Team

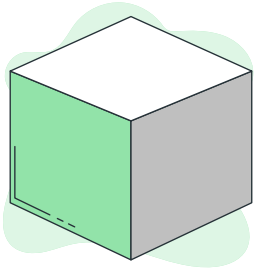
Daniel Weber, *Ahmad Ibrahim*, *Hamed Nemati*, **Michael Schwarz**, *Christian Rossow*

Transynther Research Team

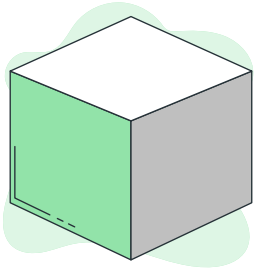
Daniel Moghimi, **Moritz Lipp**, *Berk Sunar*, **Michael Schwarz**

MSRevelio Research Team

Andreas Kogler, **Daniel Weber**, *Martin Haubenwallner*, **Moritz Lipp**, *Daniel Gruss*, **Michael Schwarz**

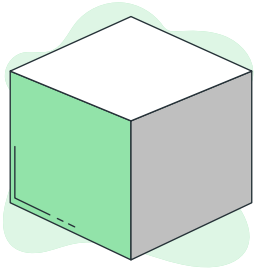


CPU



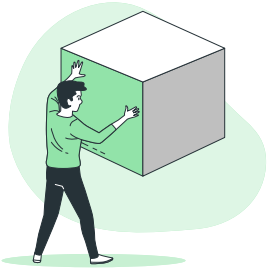
CPU

Specification (ISA)



CPU

Specification (ISA)



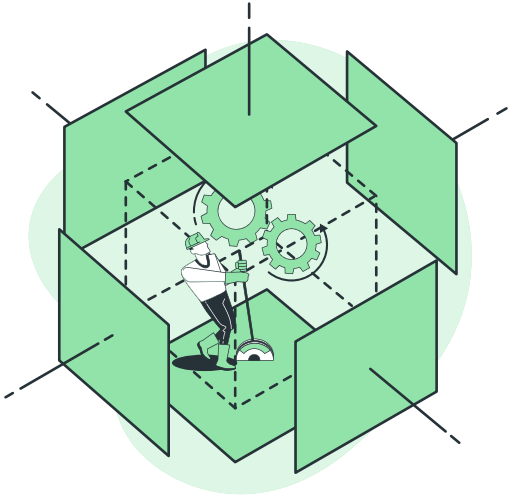
Interaction

Everything **works**
as expected

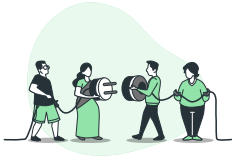
Everything **works**
as expected

No bugs

How can you attack this?



Information **leaks** through **side effects**



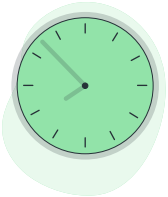
Power Consumption

Power Consumption

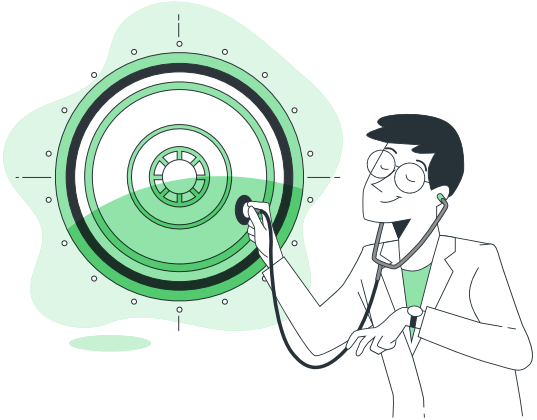
Temperature

Power Consumption

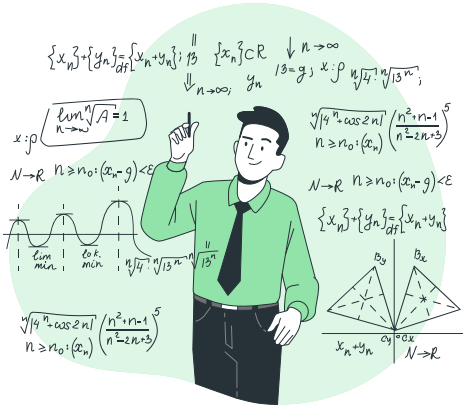
Temperature



Execution Time



Observe Device

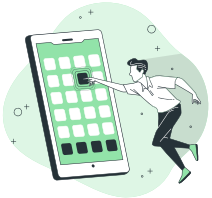


Evaluate data

Get the secrets. **Easy as that!**

Reality **is not** as easy

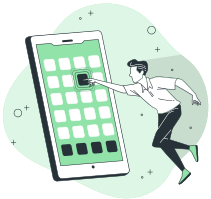
Properties



Software-only

No Physical Access required

Properties



Software-only

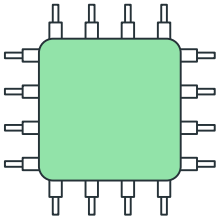
No Physical Access required

Understand Inner Workings

of the CPU

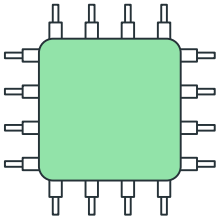
What can we observe? How does a CPU work internally?

Architecture vs Microarchitecture



- Instruction Set Architecture (ISA) is an **abstract model** of a computer (x86, ARMv8, SPARC, . . .)

Architecture vs Microarchitecture



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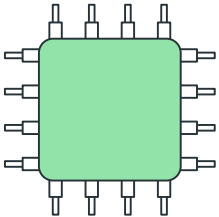
- **Interface** between hardware and software

Architecture vs Microarchitecture



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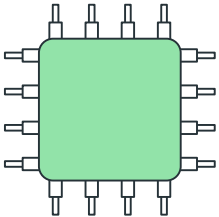
- Microarchitecture is an ISA **implementation**

Architecture vs Microarchitecture



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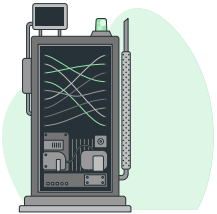
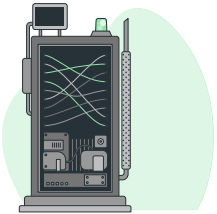
●●●

Optimizations



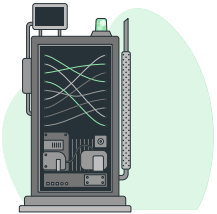
- Modern CPUs contain multiple **microarchitectural elements**

Optimizations



- Modern CPUs contain multiple **microarchitectural elements**
- **Transparent** for the programmer

Optimizations

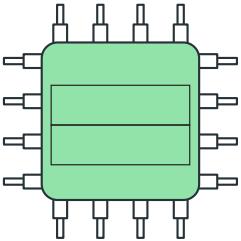


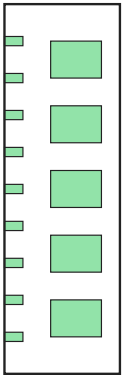
- Modern CPUs contain multiple **microarchitectural elements**
- **Transparent** for the programmer
- **Optimize** for performance, power consumption, ...

CPU Optimization: Cache

```
printf("%d", i);

printf("%d", i);
```





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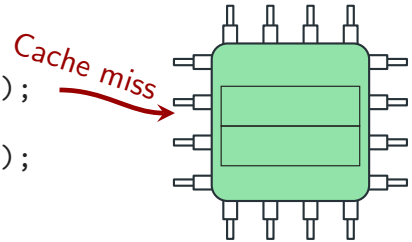

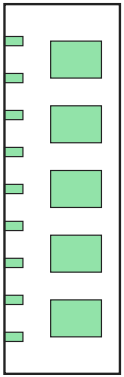

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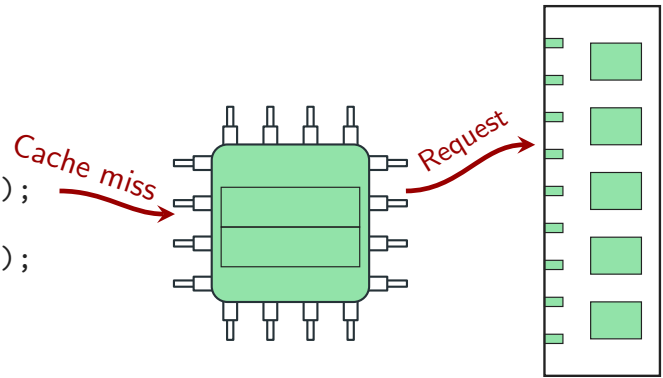

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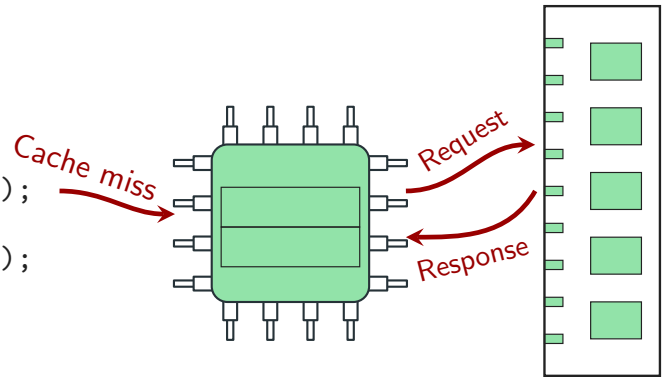

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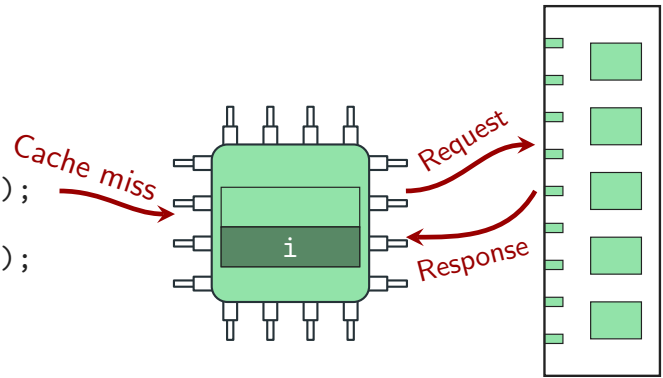
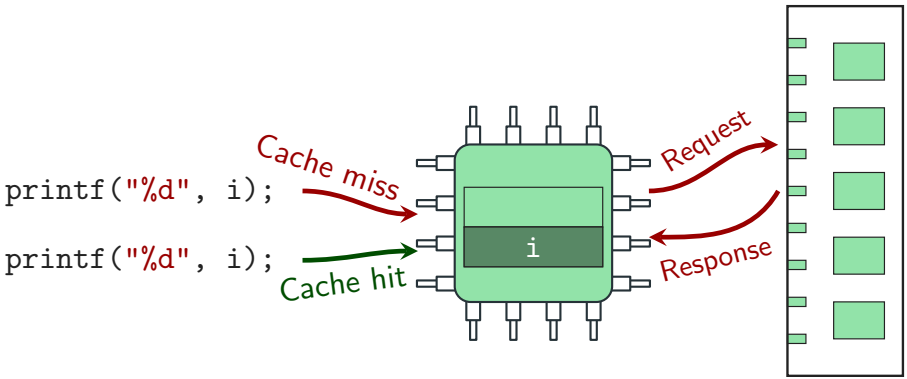


CPU Optimization: Cache



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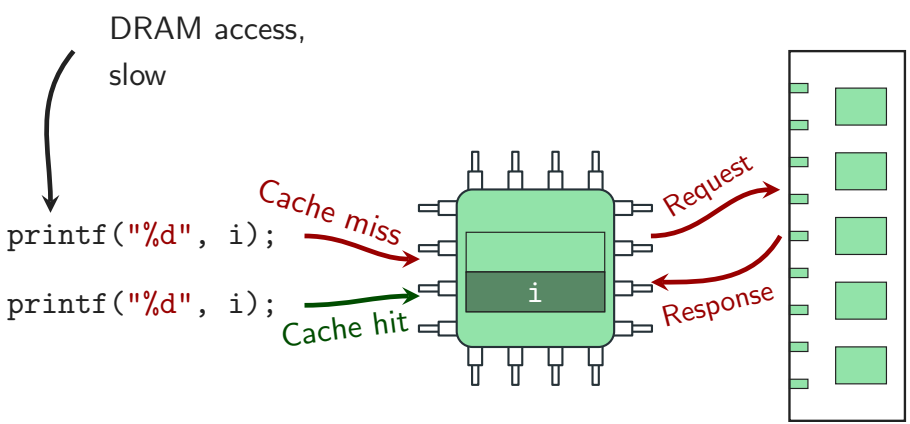
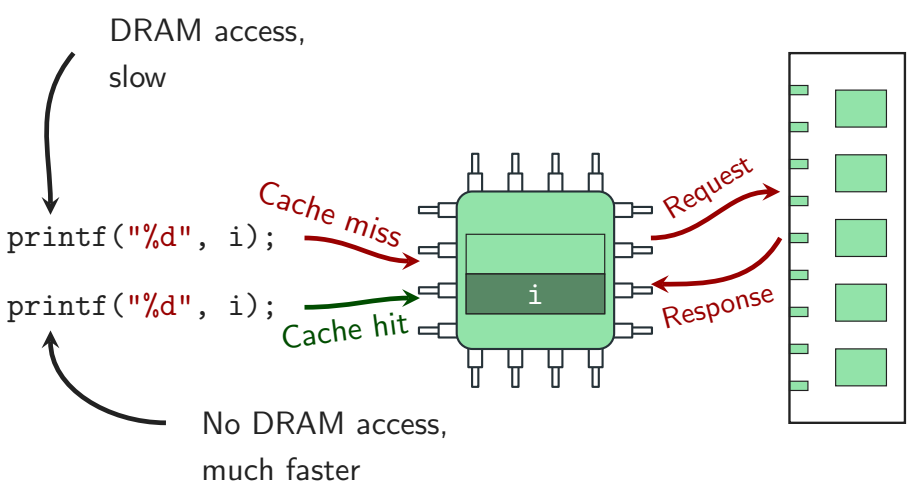
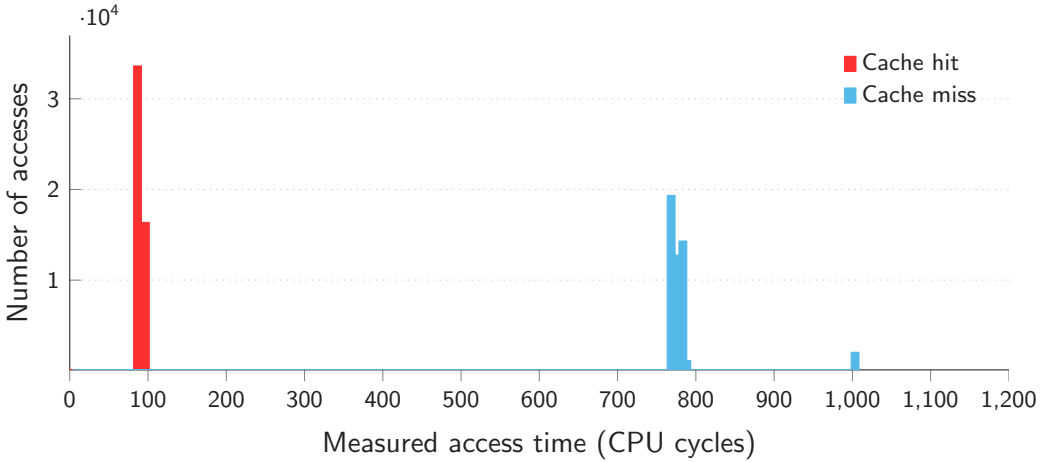


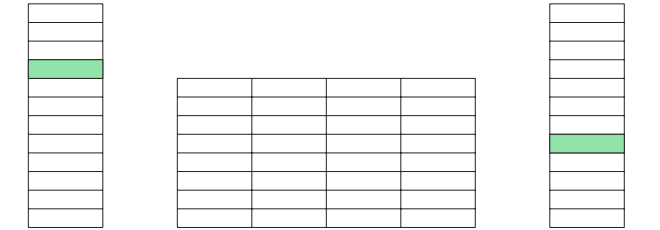
CPU Optimization: Cache



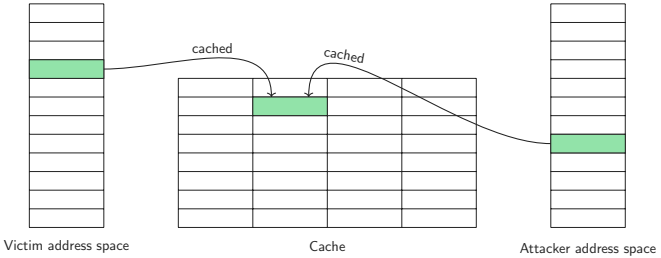
Caching speeds up Memory Accesses



Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)



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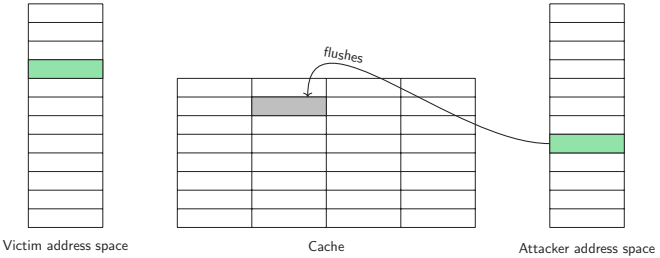
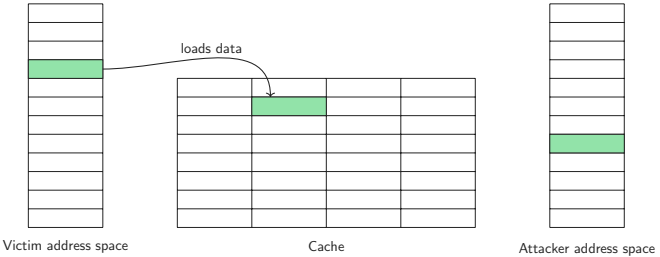


Step 1: Attacker maps shared library (shared memory, in cache)

Step 2: Attacker **flushes** the shared cache line

Flush+Reload



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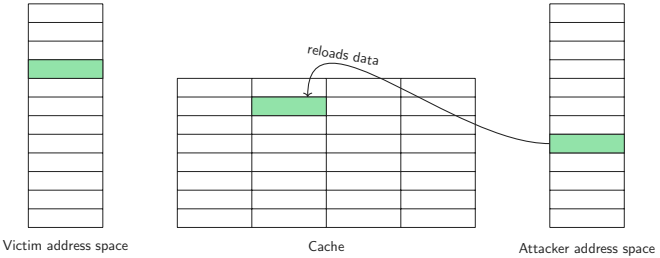
Step 2: Attacker **flushes** the shared cache line

Step 3: Victim loads the data

Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)

Step 2: Attacker **flushes** the shared cache line

Step 3: Victim loads the data

Step 4: Attacker measures the access time to **reload** the data

Cache Attacks

- Leak **cryptographic keys**

Cache Attacks

- Leak **cryptographic keys**
- Leak information on **co-located virtual machines**

Cache Attacks

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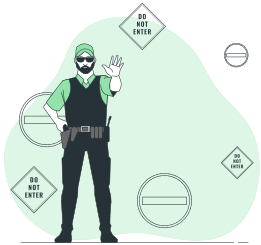
- **Monitor** function calls of **other applications**

Cache Attacks

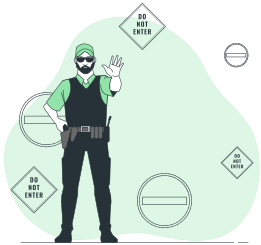
- Leak **cryptographic keys**
- Leak information on **co-located virtual machines**
- **Monitor** function calls of **other applications**
- Build **covert communication channels**
- ...

Motivation

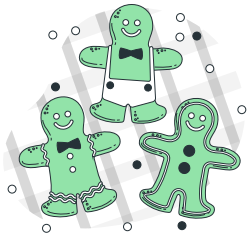


Leakage of **1** Instruction

Motivation



Leakage of **1** Instruction



There are >**3000** instructions

How do you find **these** attacks?

Read documentation and patents

Read documentation and patents

Develop ideas

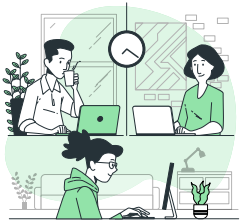
Read documentation and patents

Develop ideas

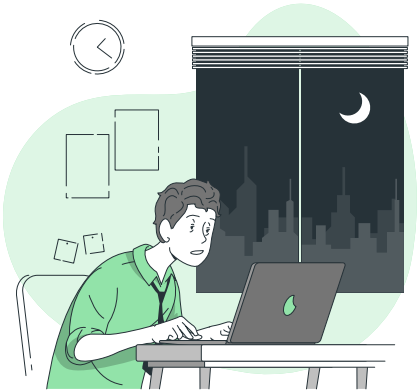
Test ideas and start over

New CPU, **New** Features

New CPU, **New** Features



Repeat from the beginning



Finding side channels and vulnerabilities is a **complex** and **time-consuming** process

Can we do **better**?

Automation for Side-Channel Search

- How can you find bugs in **software** in an automated way?

Automation for Side-Channel Search

- How can you find bugs in **software** in an automated way?
- **Fuzzing** is an automated software testing method
  - Inject invalid, malformed, unexpected input to a program

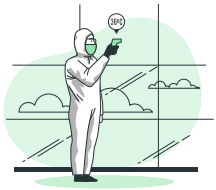
Automation for Side-Channel Search

- How can you find bugs in **software** in an automated way?
- **Fuzzing** is an automated software testing method
  - Inject invalid, malformed, unexpected input to a program
- Can we **apply a similar approach** do find microarchitectural side-channels?

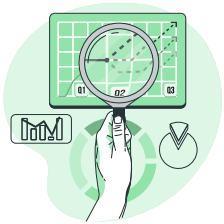
Challenges when Fuzzing CPUs

Limited Feedback

Challenges when Fuzzing CPUs

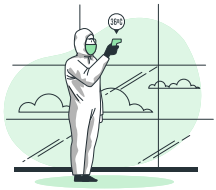


Limited Feedback

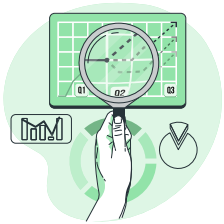


Dirty States

Challenges when Fuzzing CPUs



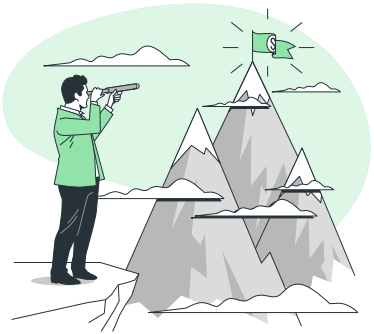
Limited Feedback



Dirty States

System Noise

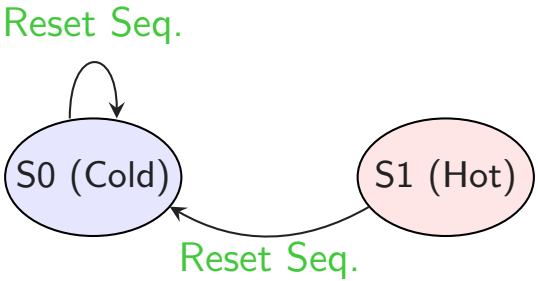
Side Channel Search



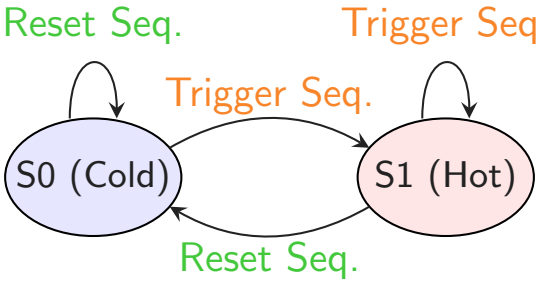
Can we **automatically decide** whether we **found a side channel?**

Modelling Side Channels

Modelling Side Channels



Modelling Side Channels



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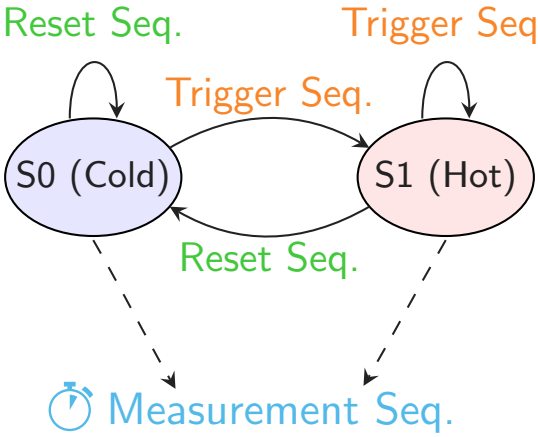

Testing Potential Side Channels

Testing Potential Side Channels

Testing Potential Side Channels

Seq_{reset}

$Seq_{measure}$

Cold path S0

Testing Potential Side Channels

Seq_{reset}

$Seq_{measure}$

Cold path S0

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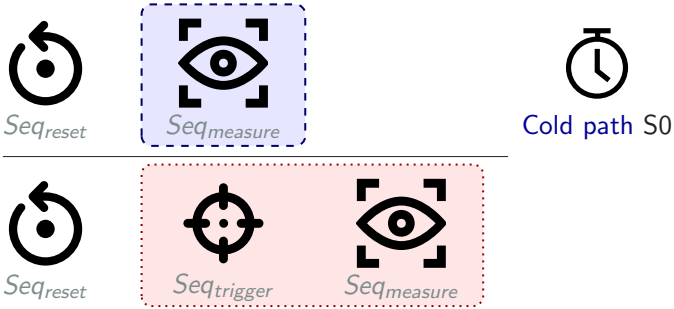
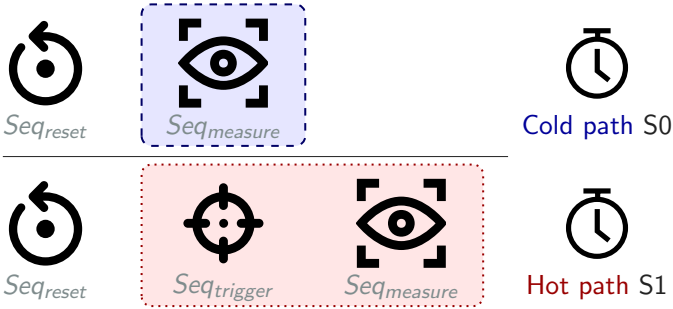
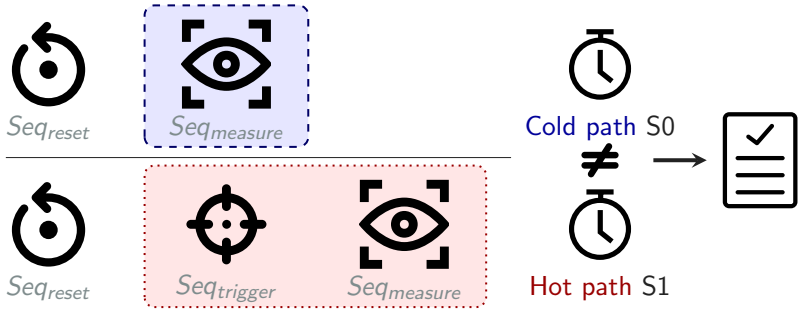
Testing Potential Side Channels



Testing Potential Side Channels

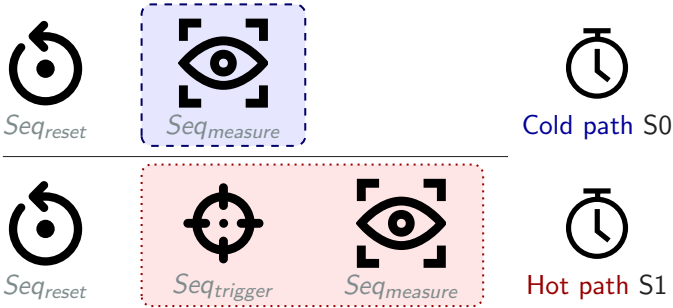


Testing Potential Side Channels



Testing Potential Side Channels

Example 1: $Seq_{measure} = Seq_{trigger} = Seq_{reset} =$ `INC [mem]`



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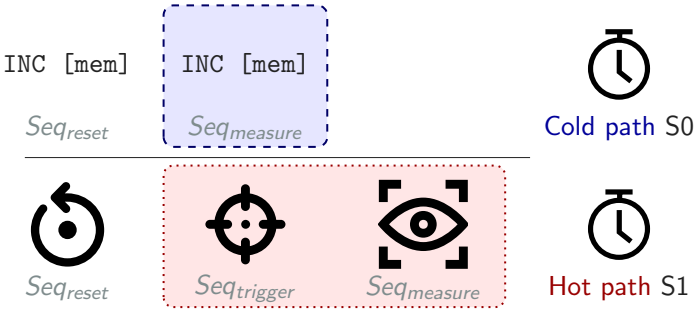

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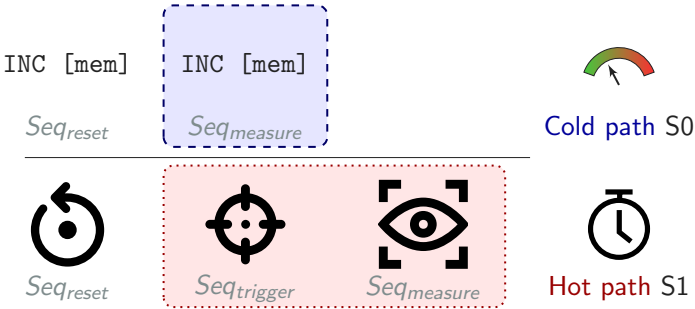

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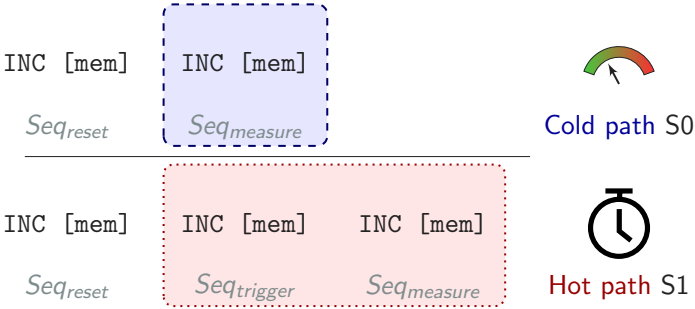

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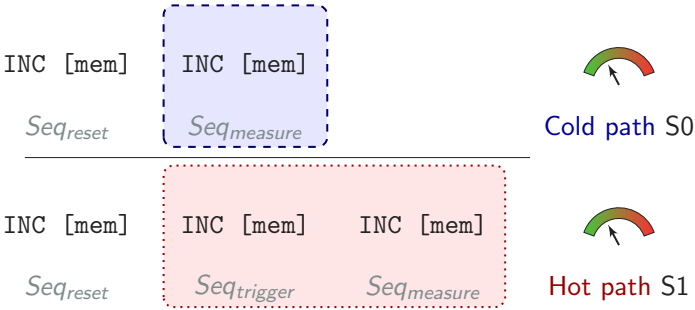

Testing Potential Side Channels

Example 2: $Seq_{measure} = Seq_{trigger} =$ `INC [mem]`;
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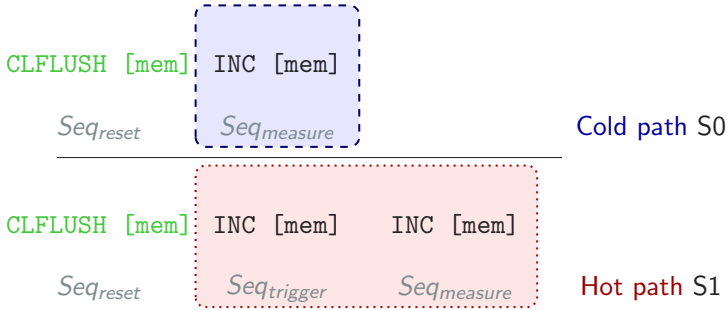

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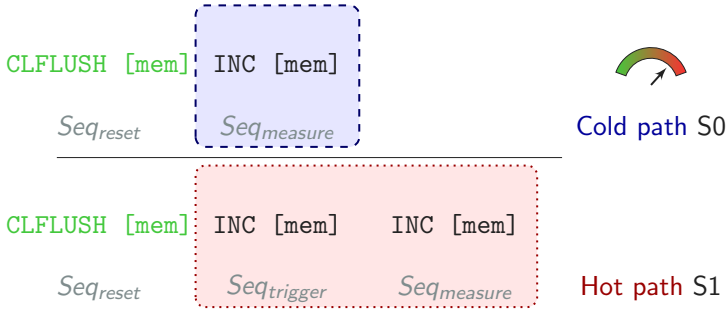

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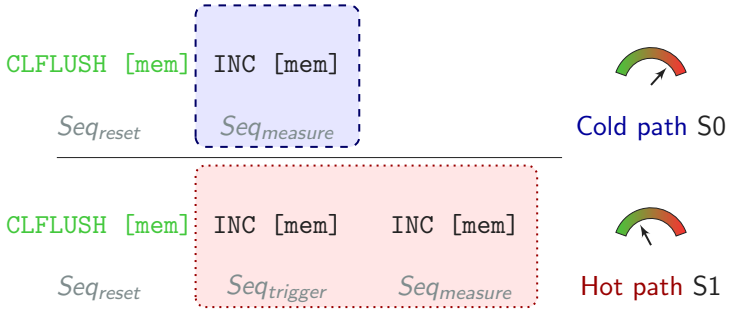

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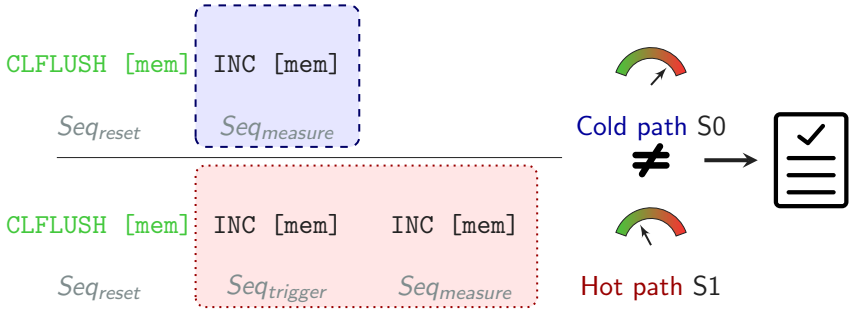
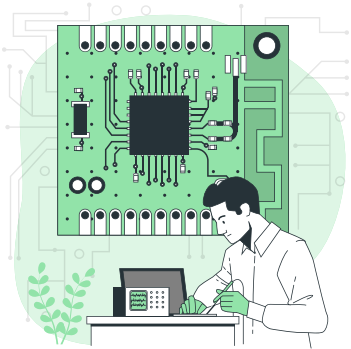
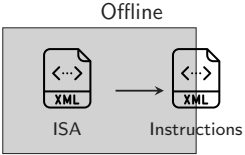




Let’s fuzz for Side Channels

Osiris – Fuzzing x86 CPUs for Side Channels



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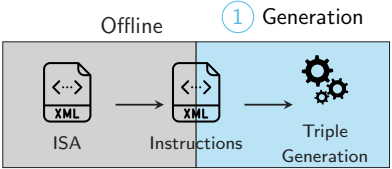

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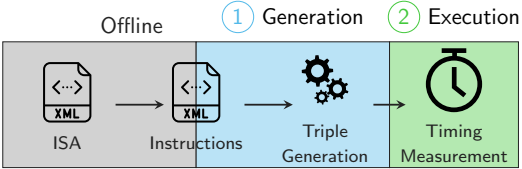

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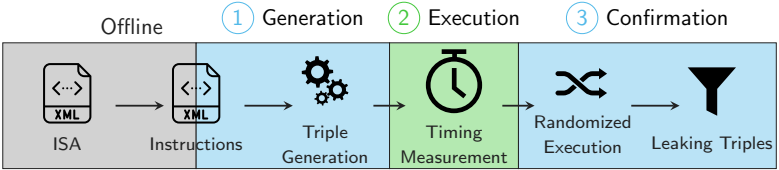

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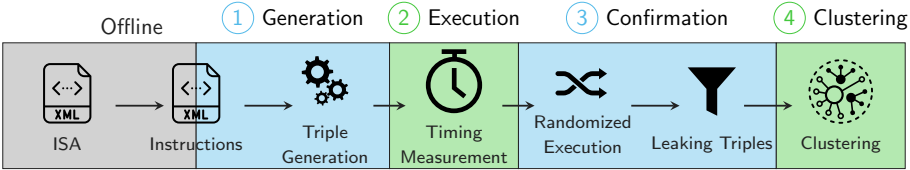
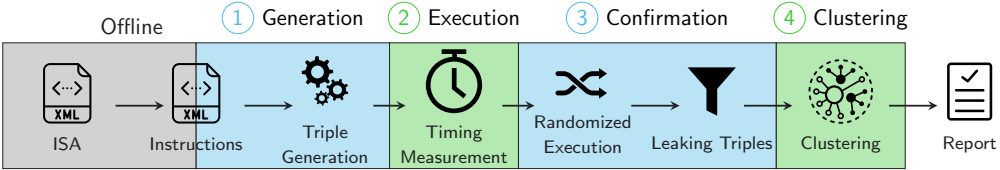


Osiris – Fuzzing x86 CPUs for Side Channels



Osiris – Results Overview

4 days

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2 side channels reproduced

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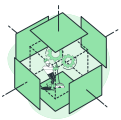
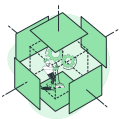


4 new side channels

Osiris – Results Overview

4 days

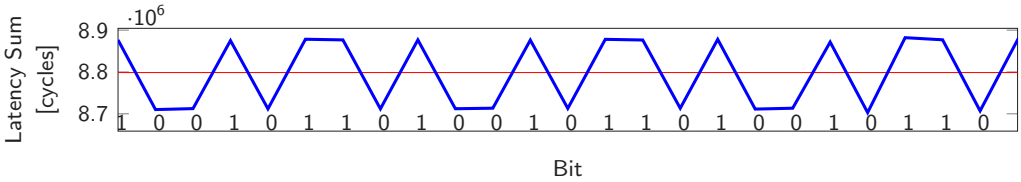
2 side channels reproduced



4 new side channels

1 new attack

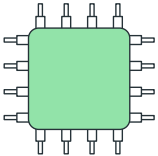
Findings – RDRAND Covert Channel



- RDRAND **cross-core** interference

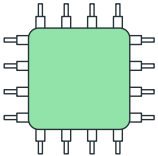
→ **Cross-core cross-VM** covert channel

Findings – RDRAND Covert Channel



AMD and Intel

Findings – RDRAND Covert Channel



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VM and native

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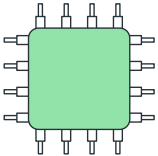

AMD and Intel

VM and native

1000 bit/s

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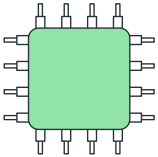


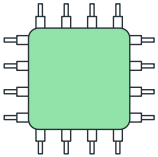
AMD and Intel

VM and native

1000 bit/s

No memory

Findings – RDRAND Covert Channel



AMD and Intel

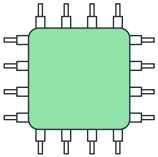
VM and native

1000 bit/s

No memory

No detection

Findings – RDRAND Covert Channel



AMD and Intel

VM and native

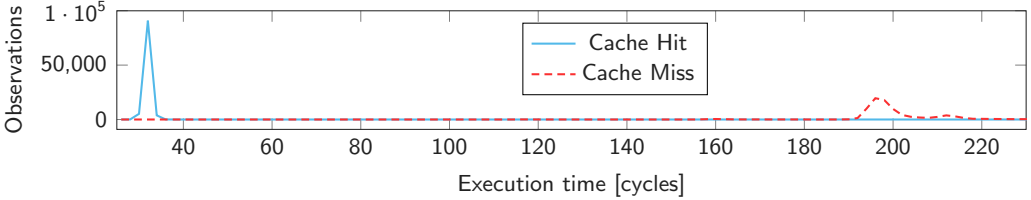
1000 bit/s

No memory

No detection

No mitigation

Findings – MOVNT Side Channel



- `MOVNT` can **replace** `CLFLUSH`
  - Flushes data from all cache levels

Findings – MOVNT Side Channel

Faster reload

Findings – MOVNT Side Channel

Faster reload

Stealthy

Findings – MOVNT Side Channel

Faster reload

Stealthy

Not prevented by any cache design

Kernel ASLR (KASLR)

- Many exploits rely on the **knowledge of the memory location** of a certain function

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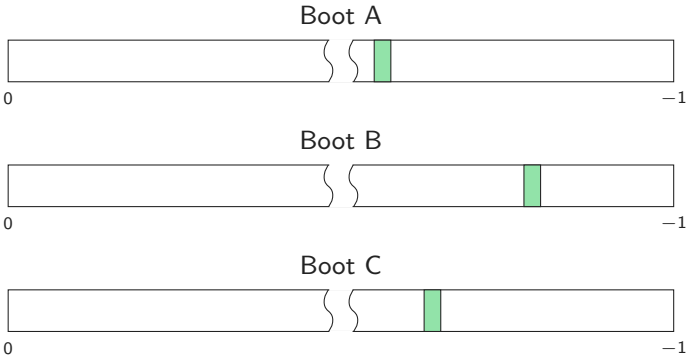
Kernel ASLR (KASLR)

- Many exploits rely on the **knowledge of the memory location** of a certain function
- OS Kernels are **protected by KASLR**
- Memory location of the kernel is **randomized**
- Attacker **do not know where** to attack

KASLR: Kernel Address Space Layout Randomization



- Kernel is loaded to a different offset on every boot

Findings – FlushConflict

- **KASLR break** based on MOVNT and transient execution

Findings – FlushConflict

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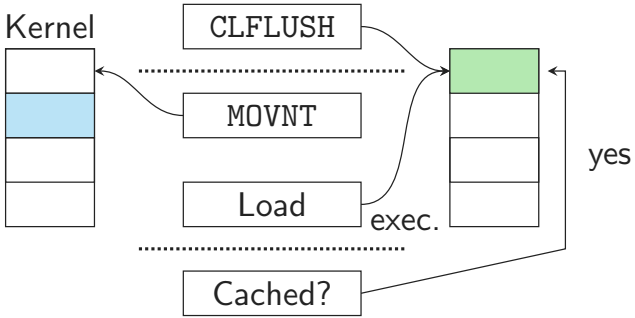
- Works **on new Intel CPUs** (tested up to Tiger Lake)

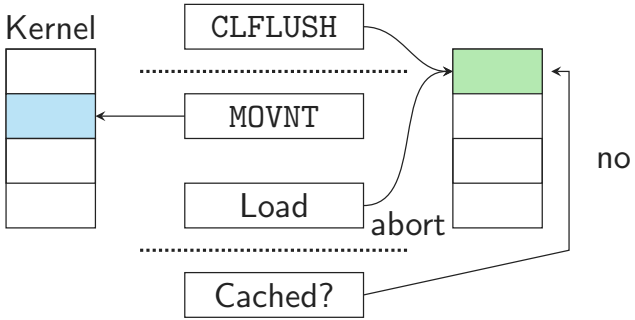
Findings – FlushConflict

- **KASLR break** based on MOVNT and transient execution
- Works **on new Intel CPUs** (tested up to Tiger Lake)
- Breaks KASLR reliably in **136ms (average)**

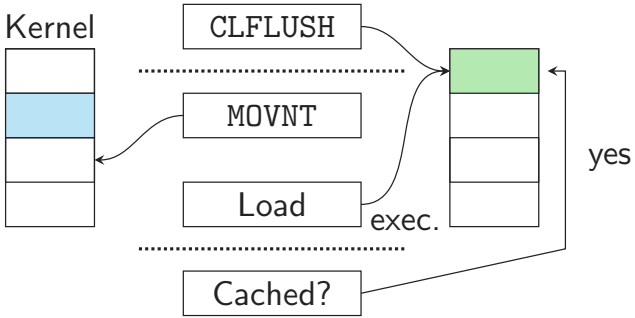
Findings – FlushConflict



Findings – FlushConflict



Findings – FlushConflict



FlushConflict Live Demo

Osiris – Lessons Learned

- We can **automatically search** for side channels

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- **Scaling** such tools is challenging

Osiris – Lessons Learned

- We can **automatically search** for side channels
- **Scaling** such tools is challenging

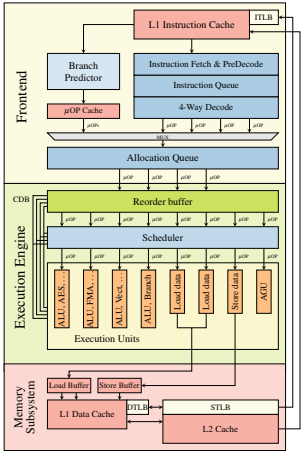
→ Osiris prototype is currently limited to 1 instruction per sequence

Can we find **more powerful attacks?**

Can we find **more powerful attacks?**

Can we **leak actual data** instead of meta data?

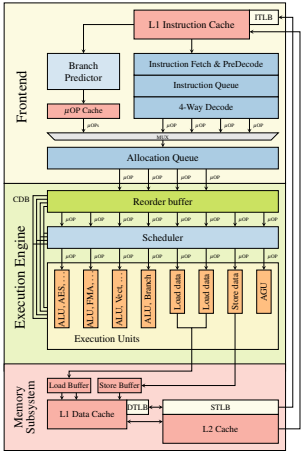
Out-of-Order Execution



Instructions are

- fetched and decoded in the **front-end**

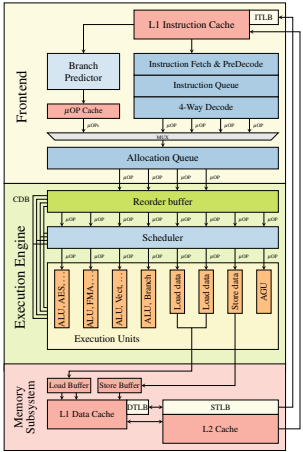
Out-of-Order Execution



Instructions are

- fetched and decoded in the **front-end**
- dispatched to the **backend**

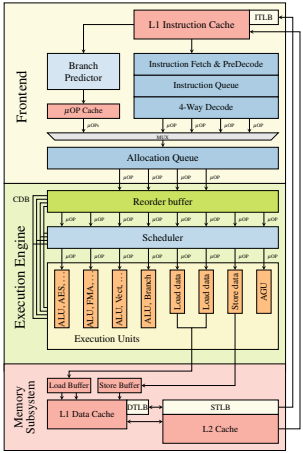
Out-of-Order Execution



Instructions are

- fetched and decoded in the **front-end**
- dispatched to the **backend**
- processed by **individual execution units**

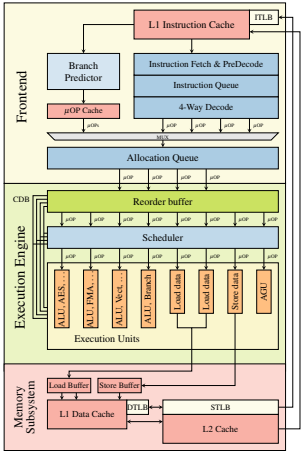
Out-of-Order Execution



Instructions

- are executed **out-of-order**

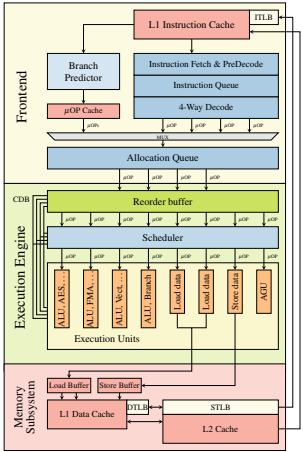
Out-of-Order Execution



Instructions

- are executed **out-of-order**
- wait until their **dependencies are ready**

Out-of-Order Execution



Instructions

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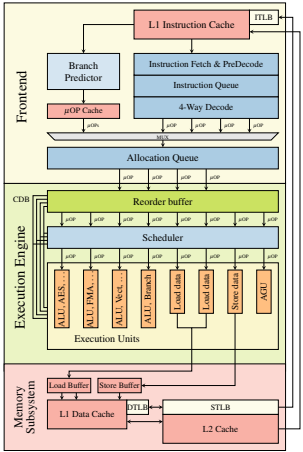
Out-of-Order Execution



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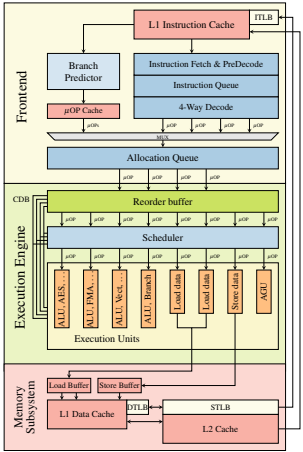
  - Later instructions might execute prior earlier instructions
- **retire in-order**

Out-of-Order Execution



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- are executed **out-of-order**
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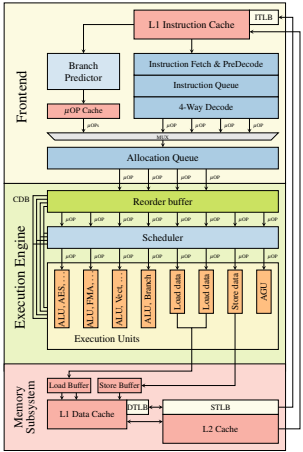
  - State becomes architecturally visible

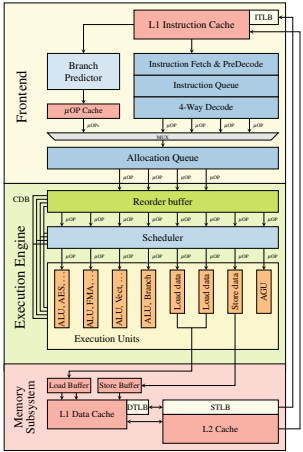
Out-of-Order Execution



Instructions

- are executed **out-of-order**
- wait until their **dependencies are ready**
  - Later instructions might execute prior earlier instructions
- **retire in-order**
  - State becomes architecturally visible
- **Exceptions** are checked during retirement

Out-of-Order Execution



Instructions

- are executed **out-of-order**
- wait until their **dependencies are ready**
  - Later instructions might execute prior earlier instructions
- **retire in-order**
  - State becomes architecturally visible
- **Exceptions** are checked during retirement
  - Flush pipeline and *recover state*

CPU Optimization: Lazy Error Handling (Out-Of-Order Execution)

- With **Meltdown**, we exploit out-of-order execution to leak the content of **inaccessible** kernel addresses

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  - → Faulty state is **never architecturally visible**
  - → Use a side-channel (Flush+Reload) to make it visible

Meltdown-type Attacks

- Many different *attack variants*
  - ZombieLoad
  - TAA
  - MDS
  - Fallout
  - ...

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- Many different *attack variants*
  - ZombieLoad
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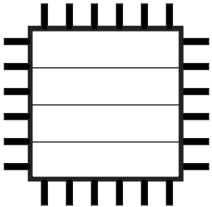
  - ...
- Leak from **different** microarchitectural buffers by triggering **different** microarchitectural conflicts

Meltdown-type Attacks

User Memory

	A	B
C	D	E
F	G	H
I	J	K
L	M	N
O	P	Q
R	S	T
U	V	W
X	Y	Z

```
char value = faulting[0]
```



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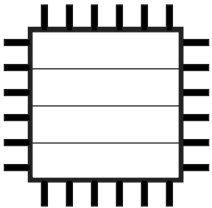

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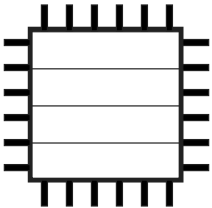
Fault

```
mem[value]
```

Out of order

K



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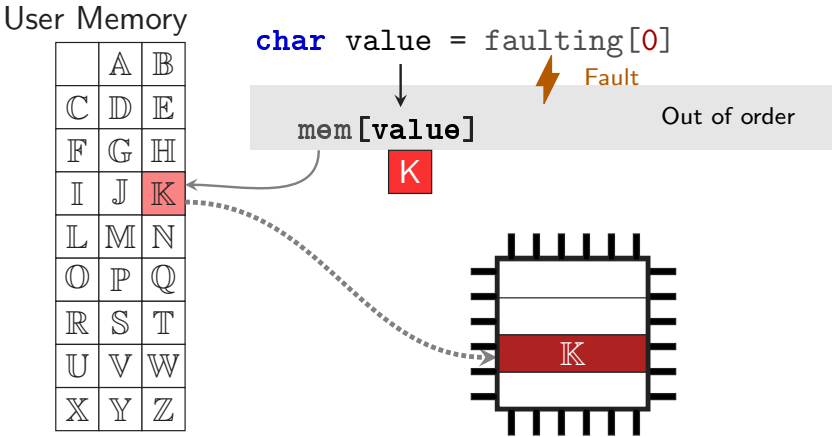

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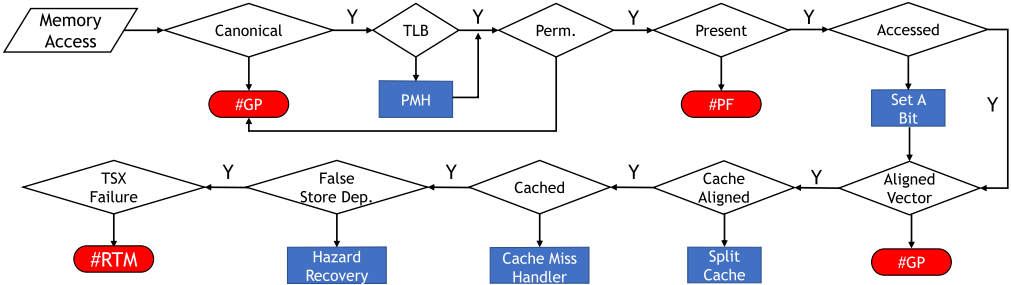
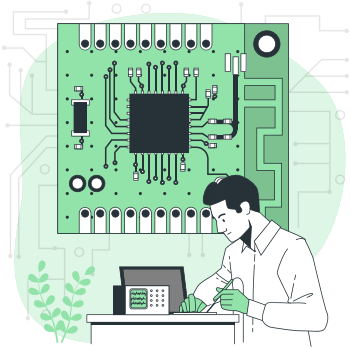
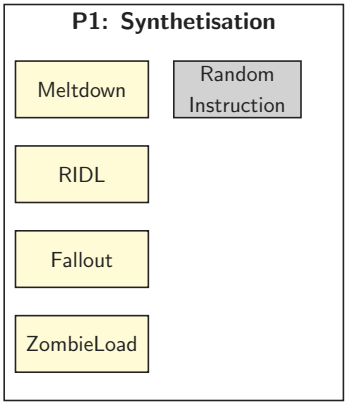




Fuzzing for Meltdown-type attacks

Transynther – Fuzzing for Meltdown-type Attacks



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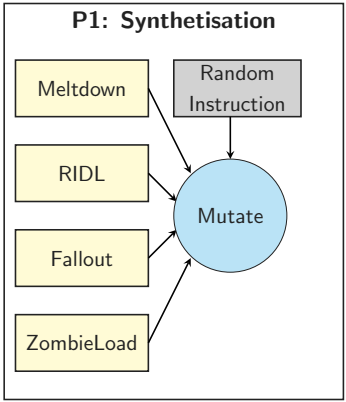

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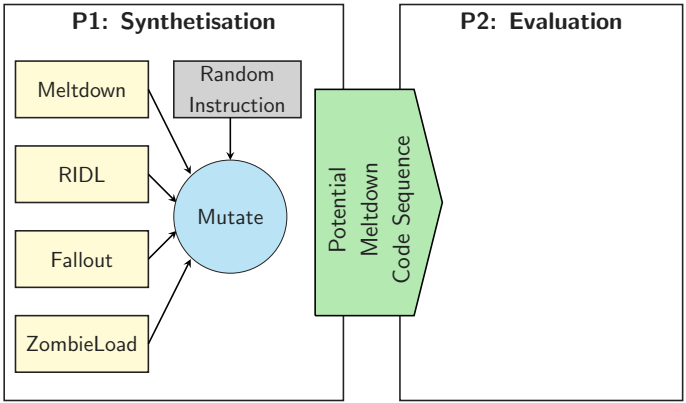

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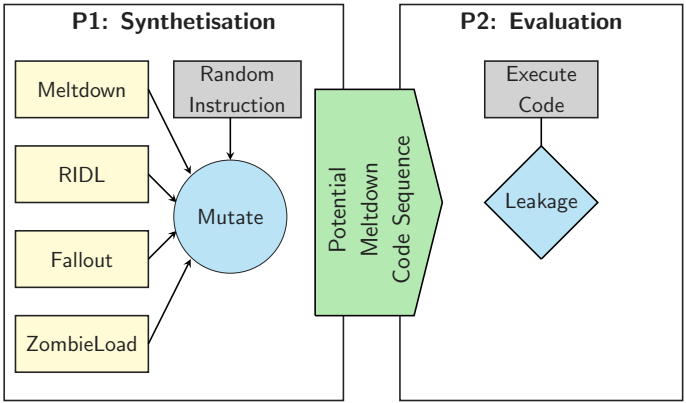

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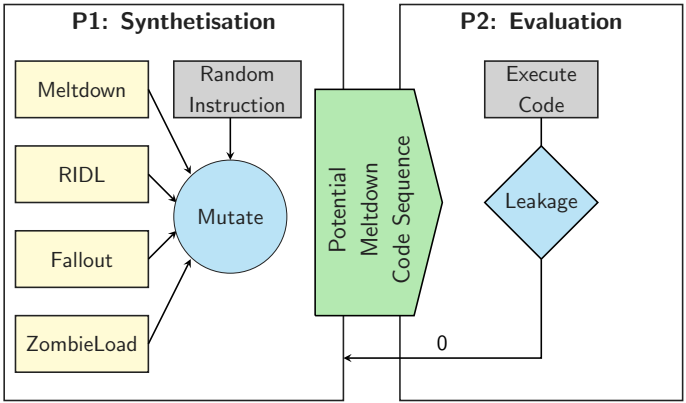

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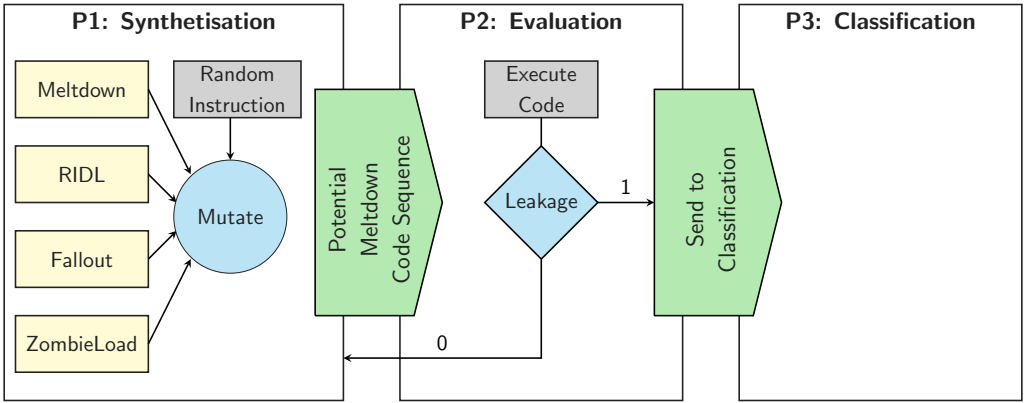
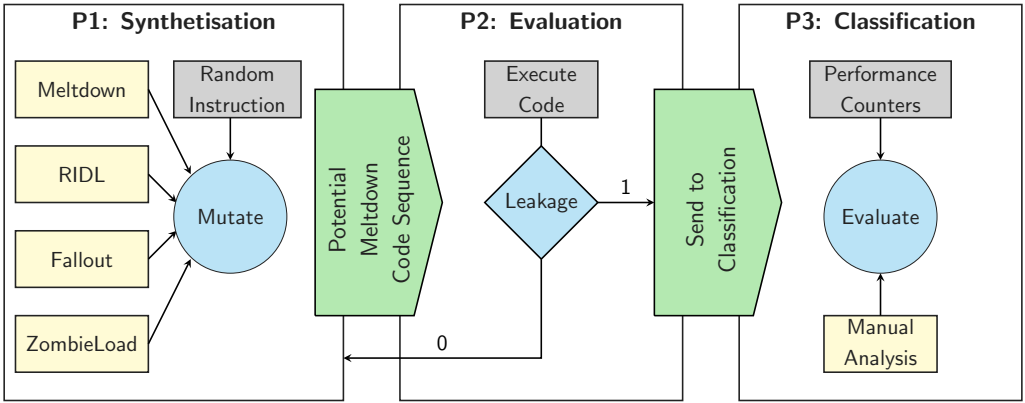


Daniel Weber, Michael Schwarz, Moritz Lipp

Transynther – Fuzzing for Meltdown-type Attacks



Transynther – Results Overview

26 hours

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Findings – Reenabling MDS Attack

- **Medusa**: new variant of **ZombieLoad**

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→ Leaked RSA key while decoding in OpenSSL

Findings – MDS Attack on Ice Lake

- Intel's Ice Lake CPUs were labeled **MDS-resistant**

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→ Transynther found a **working MDS attack**

  - Variant of a Fallout attack

Transynther – Lessons Learned

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- **Post-analysis** can also be automated
- **Regression bugs can be found** using automated tools

What about **unknown instructions**?

Finding Unknown Instructions

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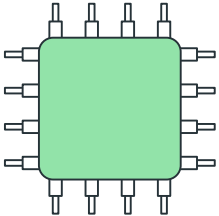
Finding Unknown Instructions

- **Sandsifter**[a] searches for undocumented x86 instructions
  - Trick to check for valid instruction bytes using page faults
- **Haruspex**[b] uses speculative execution and performance counters

[a] Sandsifter (Christopher Domas): `https://github.com/xoreaxeaxeax/sandsifter`
[b] Haruspex (Can Bölük): `https://github.com/can1357/haruspex`

What else is **left**?

Model-Specific Registers and their Hidden Secrets



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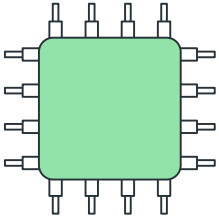
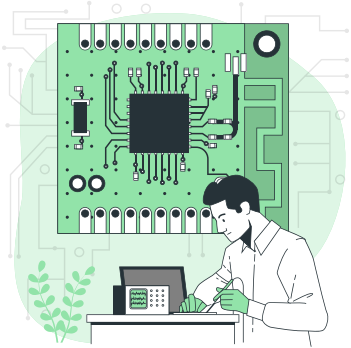
Model-Specific Registers and their Hidden Secrets



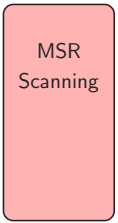
- Model-Specific Registers (MSRs) are **special CPU control registers**
- VIA C3 CPU had **backdoor access**[a] hidden behind an **undocumented MSR bit**

[a] GOD MODE unlocked: Hardware backdoors in x86 CPUs (Christopher Domas – BlackHat USA '18)



Searching for undocumented MSRs

MSRevelio – Overview



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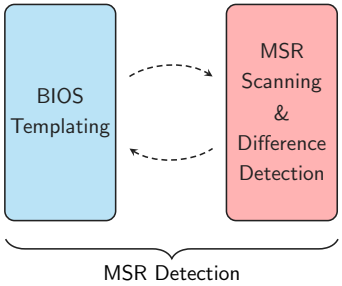

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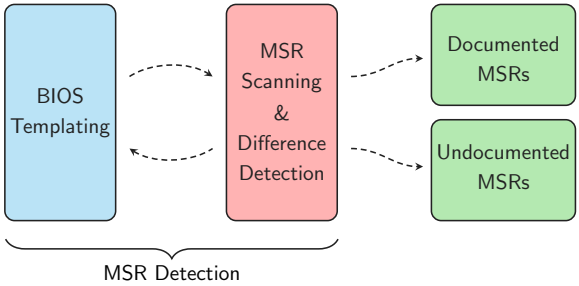

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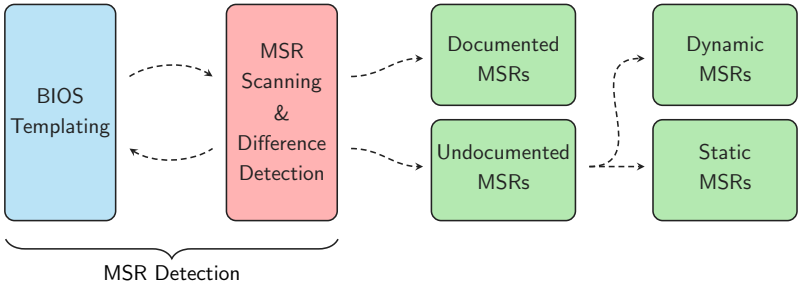

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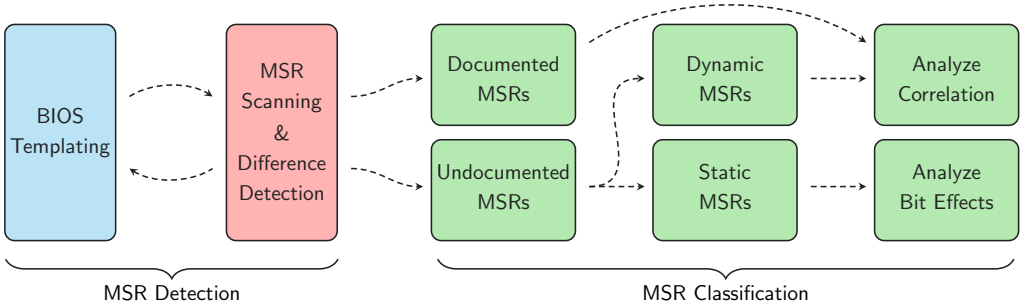

MSRevelio – Results Overview

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3 MSRs as attack **mitigation**

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New MSRs hint towards vulnerabilities

Findings – Undisclosed Attacks

- MSRs often used to introduce **vulnerability fixes**

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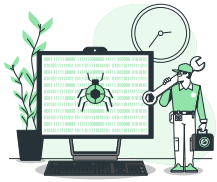
- MSRs often used to introduce **vulnerability fixes**
- MSRs exist **before public disclosure**

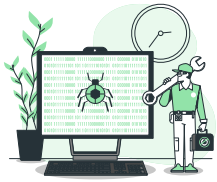
→ Useful for 1-Day Exploits

Findings – Attack Mitigation



- Mitigate **prefetch side-channel attacks**

Findings – Attack Mitigation



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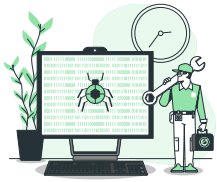

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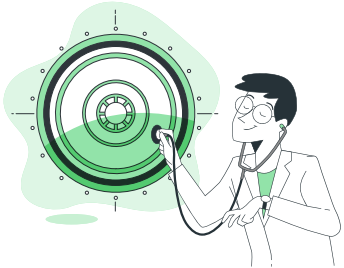
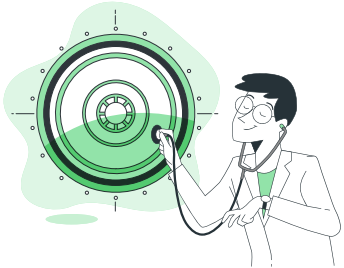
- Automation allows **tracing changes between releases** (cf. Transynther)

Conclusion



Automated **side-channel** discovery



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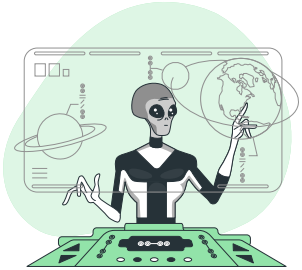

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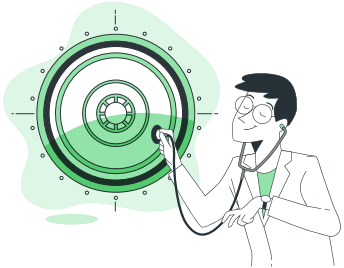

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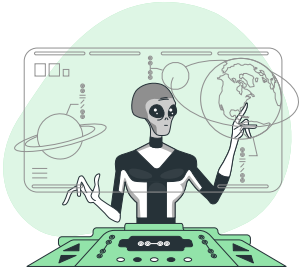

Automated **transient-execution attack** discovery

Automated detection of **undocumented MSRs**

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- **Versatile**: Execute on **various microarchitectures**

Open-Source – Feel Free to Test

All our tools are **accessible** and **open source**:

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→ `https://github.com/D4nielMoghimi/medusa`

→ `https://github.com/CISPA/osiris`

→ `https://github.com/IAIK/msrevelio`

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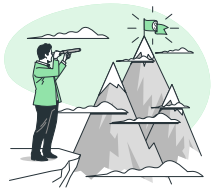

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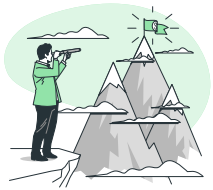

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- Play an **essential role** in CPU research

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CPU Fuzzing:
Automated Discovery of Microarchitectural Attacks

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- Icons and Images from `storyset.com`
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